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(54) Title: REFLECTIVE LAYER BURIED IN SILICON AND METHOD OF FABRICATION

(57) Abstract: A silicon wafer having a distributed Bragg reflector buried within it. The buried reflector provides a high efficiency, readily and accurately manufactured reflector with a body of silicon. A photodetector using the buried layer to form a resonant cavity enhancement of the silicon's basic quantum efficiencies and selectivity is provided. The DBR is created by bonding of two or more substrates together at a silicon oxide interface or an oxide-oxide interface. In the former, a hydrogen implant is used to cleave silicon just above the bond line. In the latter, the bonding is at the oxide layers.

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REFLECTIVE LAYER BURIED IN SILICON AND
METHOD OF FABRICATION

FIELD AND BACKGROUND OF THE INVENTION

5 The present invention was funded in whole or in part by Government Support under Contract Number DAAD17-99-2-0070 awarded by the Army Research Laboratory. The Government has certain rights in the invention.

10 The advent of high speed communications links using chains of photodetectors and emitters has increased the pressure to find a low cost, quantum efficient detector with high speed capability. Silicon has been the material of choice for such detectors. The need for sensitivity implies greater silicon thickness but that is met with increased noise and reduced bandwidth.

15 The present invention has the goal of providing a buried reflector in a silicon wafer. The buried layer has particular advantage in providing a more cost effective and efficient photodetector assembly using silicon as the light detecting material. Silicon is advantageous because its micromechanical processing is well established and understood, and thus efficient. In the construction of photodetectors of silicon it is normally desired to overcome the relatively low photon absorption of silicon through the use two reflecting surfaces separated by the silicon to provide a Fabry-Perot cavity and enhanced sensitivity and selectivity. The realization of such a cavity structure has been hampered by the fact that in conventional silicon processing, the cavity dimensions, which define selectivity and wavelength, have been hard to control.

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SUMMARY OF THE INVENTION

5 The present invention provides a reflective layer buried in silicon. The buried layer is provided as a Distributed Bragg Reflector (DBR). This reflective layer has particular advantage for use in a silicon based photodetector using resonant cavity enhancement of the silicon's basic quantum efficiencies and selectivity using the buried, distributed Bragg reflector (DBR) formed in the silicon cavity.

10 The DBR is created by bonding of two or more substrates together at a silicon oxide interface or oxide interface. In the former, an hydrogen implant is used to cleave silicon just above the bond line. In the latter, the bonding is at the oxide layers. In the former, after the steps are repeated to achieve a desired number of alternating silicon and oxide layers, a conducting layer is implanted, an epitaxial layer is grown and then another conducting implant. Finally metalizations are applied to and through the surface and a window through the oxide provided for the admittance of light.

20 In the latter case, two oxide topped wafers are joined, repeatedly to get the desired number of alternating layers. The first bonding has one layer given an implant of a dopant to impart conductivity.

DESCRIPTION OF THE DRAWING

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These and other features of the invention are more fully set forth below and in the accompanying drawing of which:

Fig. 1 is a graph illustrating the performance enhancement of a photodetector using the present invention;

5 Fig. 2 is a diagram of a photodetector structure using a buried layer according to the invention;

Fig. 3 - 24 illustrate one method of forming the buried layer and its application to a photodetector according to the present invention;

10 Figs. 25 - 31 illustrate an alternative method of forming a buried layer

Fig. 32 illustrates the invention used with on-chip electronics and optionally in an array of photodetectors.

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DETAILED DESCRIPTION

20 The present invention provides a distributed Bragg reflector (DBR) as a reflective layer in a silicon wafer. The reflective layer is shown in an application for use as a photodetector assembly. The reflective layer provides for an enhanced Fabry-Perot, resonant cavity response to incident light. The buried layer comprises alternating silicon and silicon dioxide layers
25 which form the distributed Bragg reflector (DBR).

The invention provides a buried DBR reflector which in its application to a photodetector acts to improve the quantum efficiency of a silicon light detector relative to a detector without the buried reflector.
30 Fig. 1 illustrates graphically the improvement in efficiency as a function of the buried reflectance for silicon of different α_d (absorption coefficient, silicon

depth product) values showing a great improvement over regular or conventional detectors without the buried layer. Fig. 2 illustrates the basic structure of the invention in a photodetector in which a silicon body 12 has a buried DBR layer 14 comprising alternating silicon dioxide 16 and silicon layers 18 spaced to provide a Fabry-Perot cavity in the silicon 12. To create a photodetector from the buried DBR 14 a top reflective surface is formed with the interface of the silicon 12 and the air environment.

A preferred method for the fabrication of the buried layer 14 of Fig. 2 is illustrated with respect to Figs. 3 - 13. The photodetector application is then illustrated in Figs. 11-24. In Fig. 3 a wafer of silicon 20 has an oxide layer 22 thereon. Dimensions are given in the figures for purposes of an example for a photodetector selected to respond selectively to light distributed around 850 nm (+/- nearly 100 nm), but the invention is not limited to any particular wavelength. In this case the silicon dioxide is 437 nm in depth. Hydrogen atoms are implanted through the oxide to form a thin layer 25 at an exemplary depth of 611 nm with a dosage of, for example only, $2 \times 10^{16} \text{cm}^{-2}$ to $1 \times 10^{17} \text{cm}^{-2}$ and thus and thus are placed in the silicon below the oxide as shown in Fig. 4a. A second silicon body 26 is provided in Fig. 4b and the oxide layer 22 is thermally bonded onto the top of this layer 26. The thermal bonding, typically at 600 degrees C, cleaves the boundary between the hydrogen and no hydrogen containing silicon, leaving a 174 nm silicon layer 28 on top of the oxide 24 as shown in Fig. 5. Final bonding at 1000 degrees C is then performed. The top silicon layer 28

is mechanically polished to achieve the result of Fig. 6.

Additional layers are created by continuing the above process until the desired layer structure is achieved. Fig. 7 illustrates the provision of a further body of silicon 30 having an oxide layer 32 as shown in Fig. 3. Fig. 8A illustrates the addition of an hydrogen layer 34 as above which is then bonded to the layer of Fig. 6, reproduced as Fig. 8B to achieve the bonded and cleaved wafer of Fig. 9. For the exemplary case of an 850 nm detector, a layering of hydrogenated silicon and oxide layers of 174 and 437 nm thickness is achieved. This can be repeated as many time as desired to achieve a multilayered DBR 35 shown in Fig. 10, but a DBR of two oxide layers (1.5 pairs of silicon and silicon dioxide) has been found to be an advantageous cost/performance compromise. The top layer 34 is typically mechanically polished in producing the final wafer of Fig. 10.

The top silicon layer 34 is implanted or otherwise provided with a n+ arsenic doping to provide an n-type semiconductivity to it. On top of it an epitaxial layer 36 is grown, for example, to a depth of 4,826 nm, Fig. 12, and a top layer 38 is oxidized to a depth of 500nm, Fig. 13. Because of the silicon expansion upon oxidation, this leaves 5 μm of silicon.

The invention thus shown has advantage in being able to produce uniform and accurate thickness of the buried layers insuring uniformity of performance of different units. The silicon body can also be manufactured as a single crystal layer as can the intervening silicon layers be made single crystal avoiding optical effects at crystal interfaces. The technique provided above also uses silicon fabrication

techniques which are well established and understood. The invention also can create thicknesses of widely varying relative thickness between the insulator and silicon layers. In particular it is desirable for
5 optimal reflectivity to have them of the same optical path length as above. It is thus possible to achieve high efficiency reflectance with a minimum of layers as discussed elsewhere.

The fabrication of a photodetector using the buried
10 layer of the invention is now illustrated in Figs. 14 - 24. Thereafter, and as shown in Fig. 14, the oxide layer 38 is apertured by any well known procedure to expose a surface region 40 of the detector for the admittance of light and a p+ region 42 of dopant created
15 to complete the electrode structure.

To provide electrical connection to the regions 34 and 42, the oxide layer 38 is regrown across the entire detector, Fig. 16, and a small aperture 44 off to the side of the region 42 opened in it. A deep etch 46 is
20 made to a level 48 just above the n+ layer 34, Fig. 18. An n+ dopant is implanted in the region 50 between the opening 46 and the n+ layer 34, as shown in Fig. 20. Next an entire top layer 52 of oxide is grown or otherwise formed on the surface, Fig. 21, and then
25 etched to open accesses 56 and 54 to the regions 50 and 42 respectively as shown in Fig. 22. Metalizations 60 and 58 are then deposited to provide connection from the regions 50 and 42 to the surface of the oxide layer 52, Fig. 23. Finally as shown in Fig. 24, a light
30 admitting aperture 62 is etched in the oxide layer 52 in the area of region 42 creating an upper reflecting layer and completing the photodetector. A bias source 64 would be provided for operation in light detection, the

current drawn thereby being an indication of incident light.

Formation of the DBR layer may alternatively be as shown in Figs. 25 - 31. The process begins with first and second wafers as shown in Figs. 25 and 26. Each has a buried oxide layer, layers 70 and 72 respectively, which is a wafer form generally available in industry. On each, an oxide layer, layers 74 and 76, are formed, all with the exemplary dimensions given for 850 nm sensitivity and selectivity. An n+ dopant is implanted through the layer 76 into a region 80 at an exemplary density of $1 \times 10^{19} \text{ cm}^{-3}$ of the underlying silicon region 78, Fig. 27. The surface oxide is then stripped, a new oxide grown as a wet H_2O process at 950 degrees C for typically ten minutes. The layers 74 and 76 are then brought into contact, Fig. 28, and bonded while being heated to a bonding temperature, Fig. 29. The silicon is mechanically etched as by polishing to leave a thin silicon layer, Fig. 29, which is then removed along with the oxide layer 72 leaving a silicon layer 78 on top of a DBR structure, Fig. 30. A layer 84 of oxide is then created on the silicon layer 78, Fig. 31, and creation of a top layer electrode and metalization connection can proceed as before.

In Fig. 32 there is shown a silicon chip having a buried reflector device according to the invention used in a photodetector 92. On-chip electronics 94 are provided to process signals from and energize the photodetector 92 for the provision of an output signal reflecting incident light. An array of photodetectors 96 can also be provided in association with the electronics 94 to detect light in two dimensions. The individual photodetectors may have buried layers of

different dimensions tailored to respond to different frequencies of light as well.

- 5 It is to be noted that the above described examples use dimensions for wavelengths which are exemplary only and which create no limits on the invention except as claimed.

IN THE CLAIMS

1. A silicon photodetector assembly adapted for at
5 least one frequency of light comprising:
a silicon body having a light admitting surface;
a buried Distributed Bragg Reflector (DBR) located
within said body and facing said light admitting
surface;
10 semiconducting layers adjacent said light admitting
surface and said DBR respectively;
said light admitting surface and said DBR forming a
resonant cavity to said one or more frequencies of
light.
15
2. The photodetector assembly of claim 1 further
including a source of electrical bias for said assembly.
3. The photodetector assembly of claim 2 wherein said
20 semiconducting layers are of one type adjacent said
light admitting surface and of another type adjacent
said DBR.
4. The photodetector assembly of claim 3 wherein said
25 semiconducting layers are "n" type adjacent said DBR and
"p" type adjacent said light admitting surface.
5. The photodetector assembly of claim 1 wherein said
DBR includes one or more alternating layers of silicon
30 and silicon dioxide.

6. The photodetector assembly of claim 1 wherein said DBR includes 1.5 pairs of silicon and silicon dioxide layers.

5 7. The photodetector assembly of claim 1 wherein said at least one frequency is approximately 850 nm.

8. The photodetector assembly of claim 1 wherein said DBR includes layers of silicon and silicon dioxide
10 formed from different silicon wafers bonded to form said DBR.

9. The photodetector of claim 8 wherein said bonded layers are bonded at silicon and silicon dioxide
15 surfaces.

10. The photodetector of claim 1 wherein DBR includes at least one layer from an original silicon wafer layer and at least one grown layer.
20

11. The photodetector of claim 1 wherein said DBR includes at least one silicon layer cleaved from a region of hydrogen implanted atoms.

25 12. The photodetector assembly of claim 1 wherein said cavity is a Fabry-Perot cavity.

13. The photodetector assembly of claim 1 wherein said layers of silicon and silicon dioxide are respectively
30 approximately 174 and 437 nm in thickness.

14. A method for fabricating a silicon photodetector assembly adapted for one or more frequencies of light comprising the steps of:

5 providing a first body of silicon having a layer of silicon dioxide on a surface thereof;

providing a second body of silicon;

Implanting hydrogen atoms at a predetermined depth in said silicon surface forming a boundary between hydrogen implanted silicon and unimplanted silicon;

10 bonding a silicon surface of said second body to the silicon dioxide layer of the first body;

separating the hydrogen implanted silicon from silicon not hydrogen implanted at said boundary thereby exposing a separated surface;

15 providing a further body of silicon having a layer of silicon dioxide thereon;

Implanting hydrogen atoms at a predetermined depth in said further body forming a boundary between hydrogen implanted silicon and unimplanted silicon;

20 bonding the silicon dioxide layer of said further body to said exposed silicon surface;

25 separating the hydrogen implanted silicon from silicon not hydrogen implanted at said boundary of said further body thereby exposing a separated surface thereof;

providing a silicon layer on the separated surface of said further body separated by semiconducting regions to form a cavity for light.

30 15. The method of claim 14 further including the steps of repeating the last mentioned further body providing, implanting, bonding, and separating steps one or more times.

16. The method of claim 14 wherein said bonding step includes the step of heating the hydrogen implanted body to promote cleaving or fracturing at regions containing hydrogen.

17. The method of claim 16 wherein said heating step includes heating to a cleaving temperature followed by heating to a bond strengthening temperature.

18. The method of claim 17 wherein said cleaving temperatures and strengthening temperatures are respectively approximately 600 degrees C and 1000 degrees C.

19. The method of claim 14 wherein the step of providing a silicon layer includes the step of growing an epitaxial layer on the silicon fractured at said boundary.

20. The method of claim 14 wherein said step of providing a silicon layer includes the step of providing a first semiconducting layer adjacent said boundary.

21. The method of claim 20 wherein said step of providing a silicon layer includes the step of providing a light admitting second semiconductor layer at an outer surface thereof.

22. The method of claim 21 further including the step of providing conducting connections to said each of first and second layers.

23. The method of claim 22 further including the step of biasing said conducting connections.

5 24. A photodetector assembly manufactured according to the method of claim 14.

25. A method of manufacturing a photodetector assembly comprising the steps of:

10 forming alternating silicon and silicon dioxide layers;

forming a Fabry-Perot cavity adjacent to said alternating layers;

15 providing electrical contact to opposite sides of said cavity.

26. The method of claim 25 wherein said step of providing alternating layers includes providing said layers as bonded separate substrates.

20 27. The method of claim 25 wherein said step of providing alternating layers includes the step of providing hydrogen atoms therein.

25 28. A photodetector assembly manufactured according to the method of claim 27.

30 29. A reflecting layer buried within a silicon body and adapted for reflection at at least one frequency of light comprising:

a silicon body having a light admitting surface;

a buried Distributed Bragg Reflector (DBR) located within said body and facing said light admitting surface;

5 said DBR comprising alternating layers of insulator and silicon of thicknesses which are a function of said at least one frequency;

10 said silicon body extending toward said surface from said DBR with said DBR functioning to redirect light through said silicon body.

30. The buried reflecting layer of claim 29 wherein said DBR includes one or more alternating layers of silicon and silicon dioxide.

15 31. The buried reflecting layer of claim 29 wherein said DBR includes 1.5 pairs of silicon and silicon dioxide layers.

20 32. The buried reflecting layer of claim 29 wherein said at least one frequency is approximately 850 nm.

25 33. The buried reflecting layer of claim 29 wherein said DBR includes layers of silicon and silicon dioxide formed from different silicon wafers bonded to form said DBR.

30 34. The buried reflecting layer of claim 33 wherein said bonded layers are bonded at silicon and silicon dioxide surfaces.

35. The buried reflecting layer of claim 34 wherein DBR includes at least one layer from an original silicon wafer layer and at least one grown layer.

5

36. The buried reflecting layer of claim 35 wherein said DBR includes at least one silicon layer having hydrogen atoms implanted therein.

10

37. The buried reflecting layer of claim 34 wherein said layers of silicon and silicon dioxide are respectively approximately 174 and 437 nm in thickness.

15

38. The buried DBR of claim 29 wherein said insulator and silicon layer have substantially the same optical path length.

39. A method for fabricating a buried reflective layer in silicon adapted for one or more frequencies of light comprising the steps of:

providing a first body of silicon having a layer of silicon dioxide on a surface thereof;

providing a second body of silicon;

20

Implanting hydrogen atoms to a predetermined depth in said silicon surface forming a boundary between hydrogen implanted silicon and unimplanted silicon on either side thereof;

25

bonding a silicon surface of said second body to the silicon dioxide layer of the first body;

separating the silicon at the hydrogen boundary thereby exposing a separated surface;

providing a further body of silicon having a layer of silicon dioxide thereon;

30

implanting hydrogen atoms to a predetermined depth in said further body forming a boundary between hydrogen implanted silicon and unimplanted silicon on either side thereof;

bonding the silicon dioxide layer of said further body to said exposed silicon surface;

separating the silicon at the hydrogen boundary thereby exposing a separated surface.

5

40. A method for fabricating a buried reflective layer in silicon of claim 39 further including the steps of repeating the last mentioned further body providing, implanting, bonding, and separating steps one or more times.

10

41. A method for fabricating a buried reflective layer in silicon of claim 39 wherein said bonding step includes the step of heating the hydrogen implanted body to promote cleaving or fracturing of regions containing hydrogen from regions not containing hydrogen.

15

42. A method for fabricating a buried reflective layer in silicon of claim 41 wherein said heating step includes heating to a cleaving temperature followed by heating to a bond strengthening temperature.

20

43. A method for fabricating a buried reflective layer in silicon of claim 42 wherein said cleaving temperatures and strengthening temperatures are respectively approximately 600 degrees C and 1000 degrees C.

25

44. A method for fabricating a buried reflective layer in silicon claim 43 further including the step of providing a silicon epitaxial layer on the silicon fractured at said boundary.

30

45. A buried reflector assembly manufactured according to the method of claim 29.

5 46. A single silicon wafer having photolithographically formed therein a photodetector having a buried reflector according to claim 29 and a signal processing circuit connected thereto to enable the detection of light thereby.

10 47. An array of photodetectors having buried reflectors according to claim 29 and formed in a single silicon wafer and adapted to respond to light incident over said array.

15 48. The array of claim 47 wherein at least some of the photodetectors in the array have buried layers dimensioned for different frequencies.

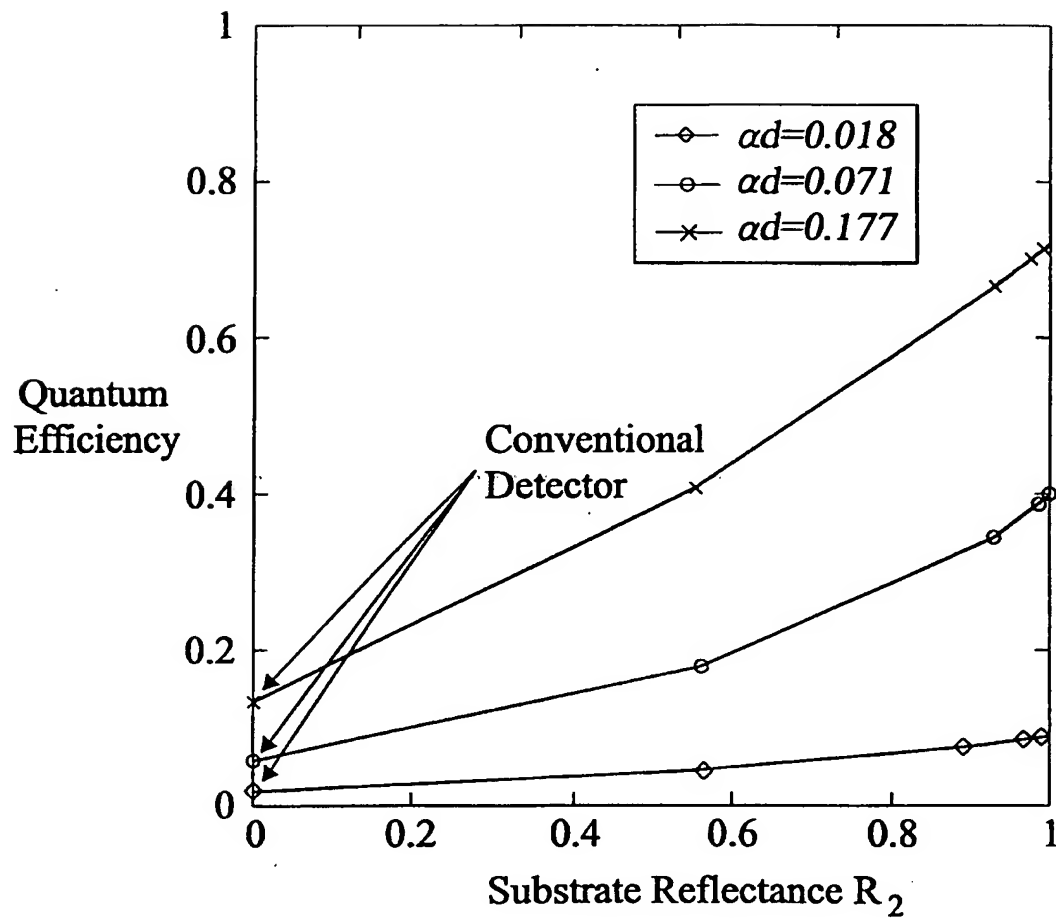
20 49. The array of claim 47 further including processing electronics formed in said array.

25 50. A photodetector having a buried DBR layer according to claim 29 and further including layers thereon selected from the group consisting of a SiGe absorption region, SiGe/Si quantum well absorption region, or metal semiconductor internal photoemission (Schottky) type absorption region using metal selected from the group consisting of Pt, Ir, Pd or Ni.

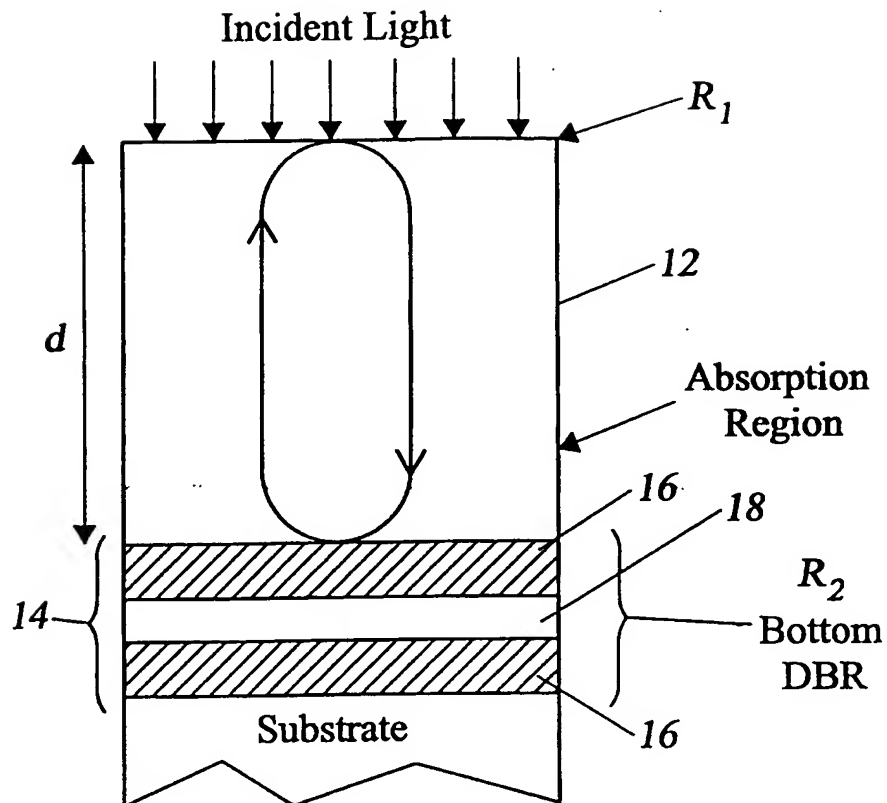
30 51. A method for manufacturing a photodetector having a buried DBR layer made according to the method of claim 39 and further including the steps of forming layers thereon selected from the group consisting of a SiGe

absorption region, SiGe/Si quantum well absorptpion region, or metal semiconductor internal photoemission (Schottky) type absorption region using metal selected from the group consisting of Pt, Ir, Pd pr Ni.

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*FIG. 1*

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**FIG. 2**

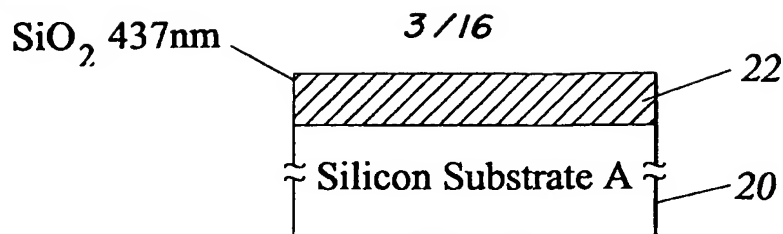


FIG. 3

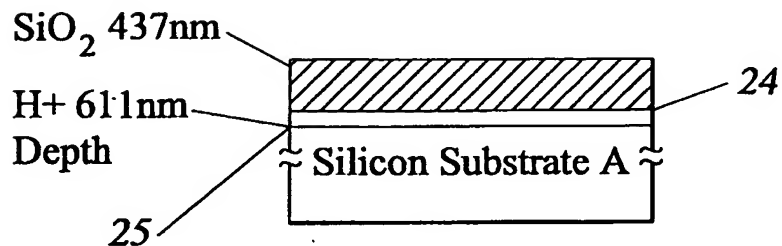


FIG. 4A

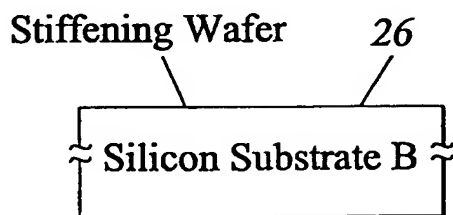


FIG. 4B

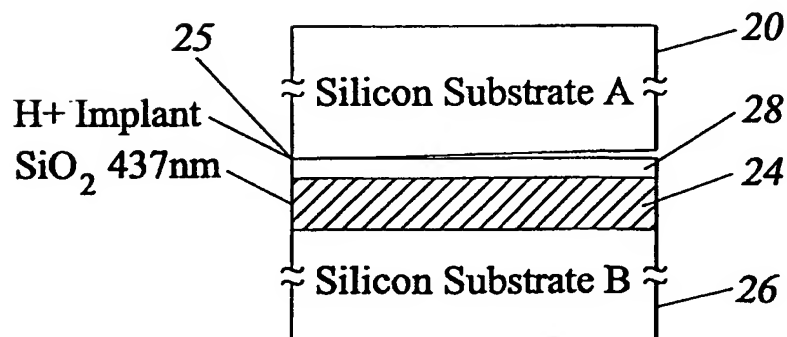
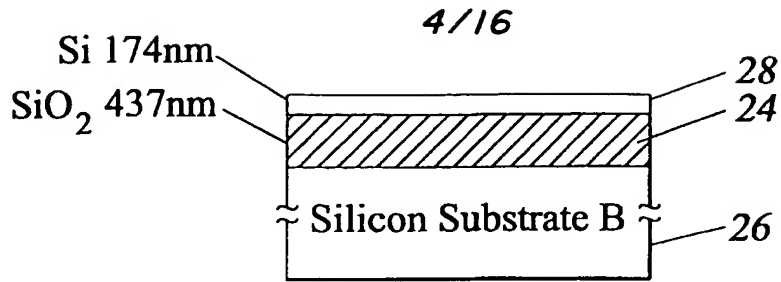
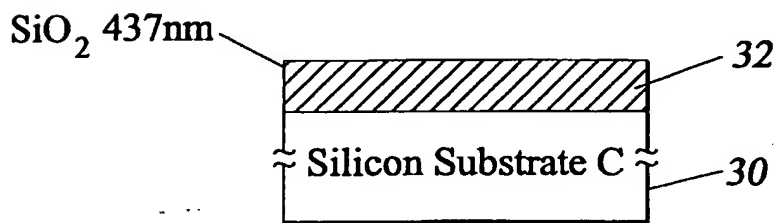
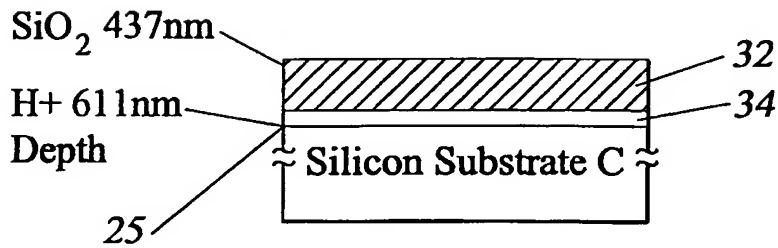
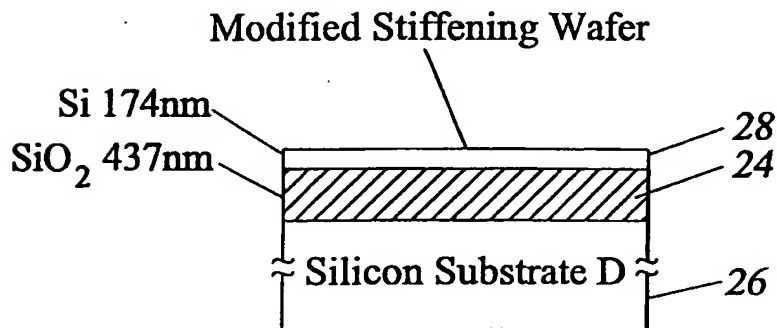


FIG. 5

*FIG. 6**FIG. 7**FIG. 8A**FIG. 8B*

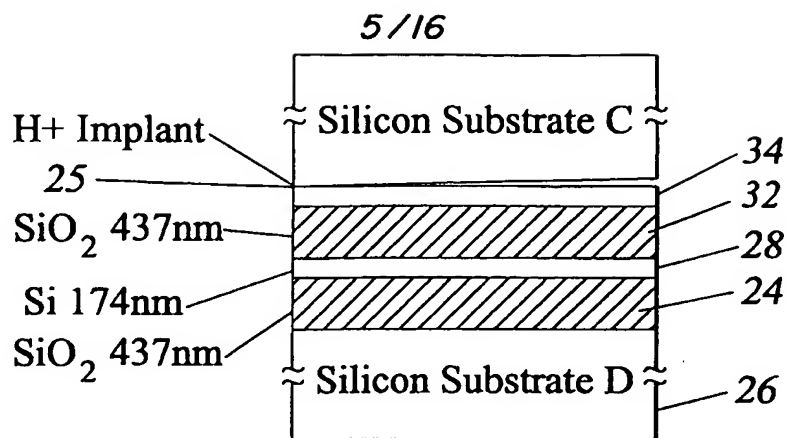


FIG. 9

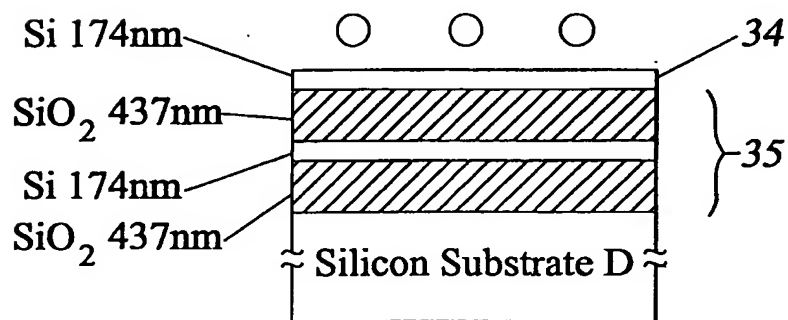


FIG. 10

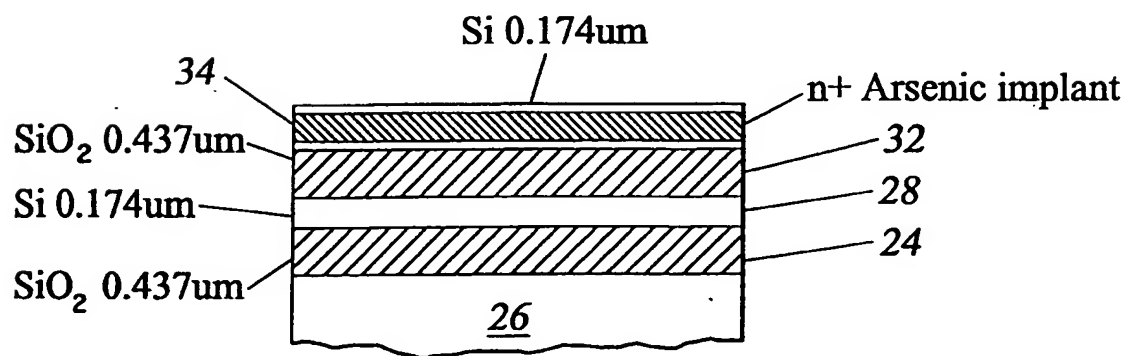


FIG. 11

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Si 4.826um/5.00um total

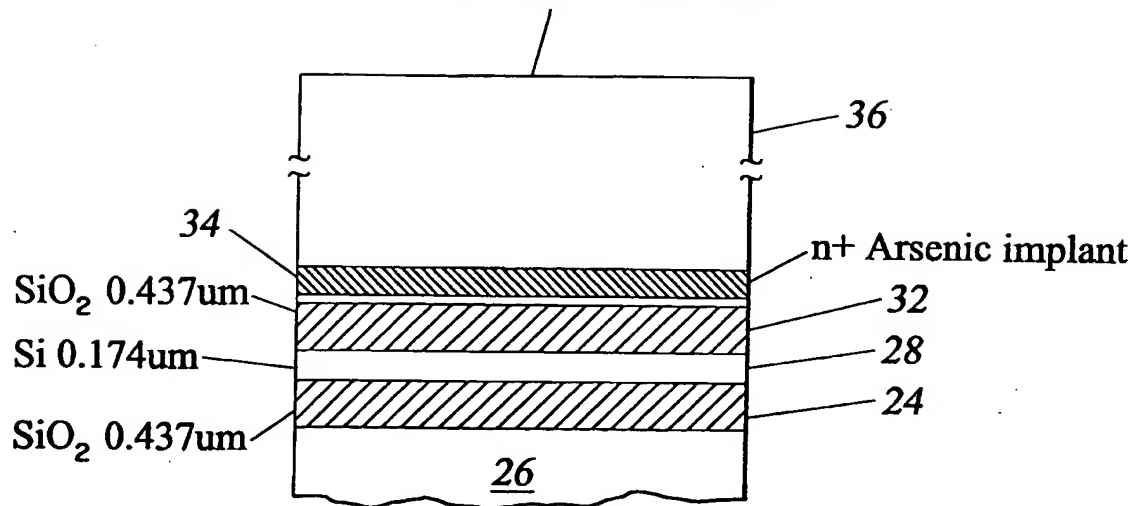


FIG. 12

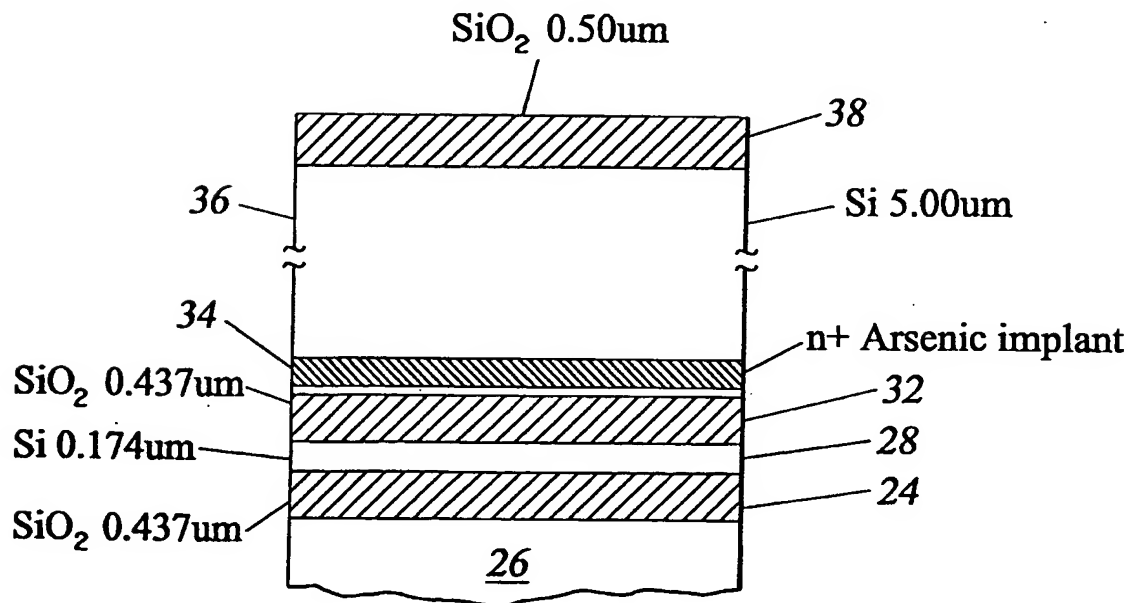
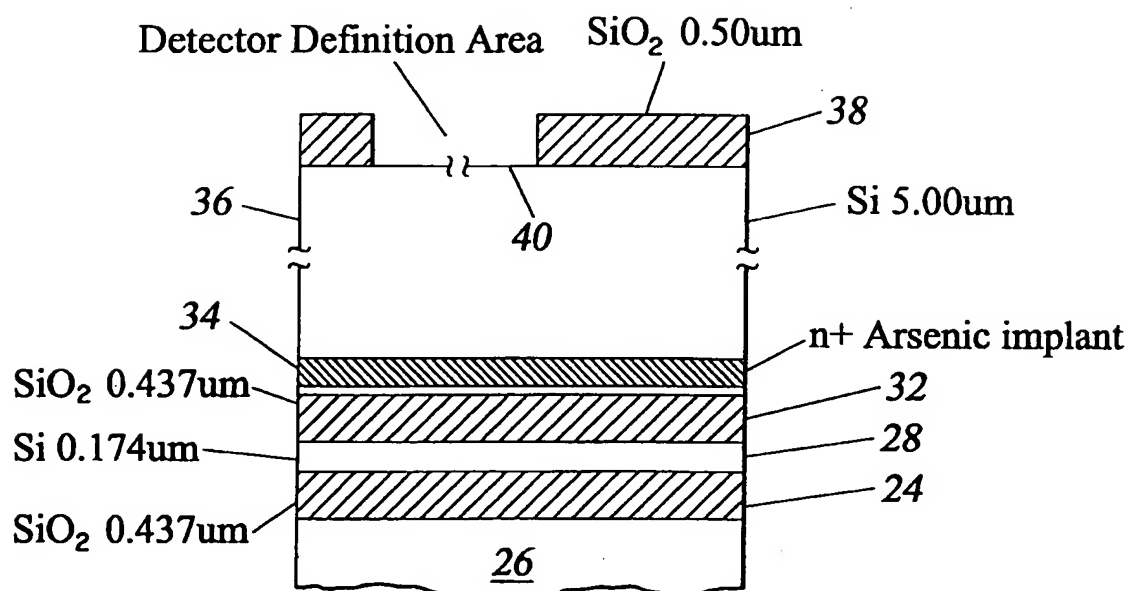
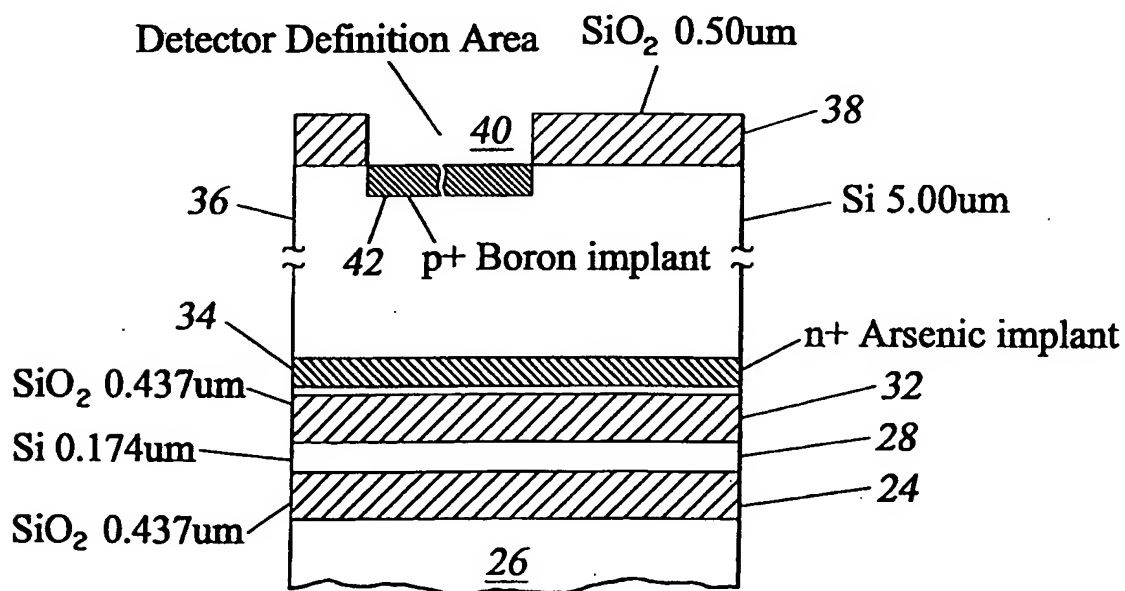
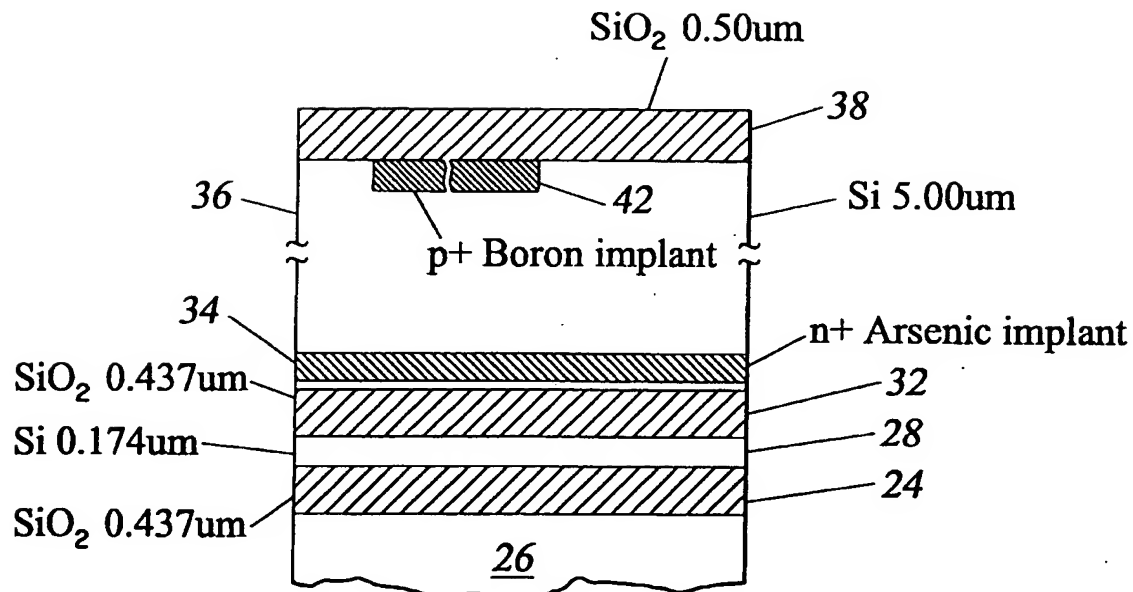
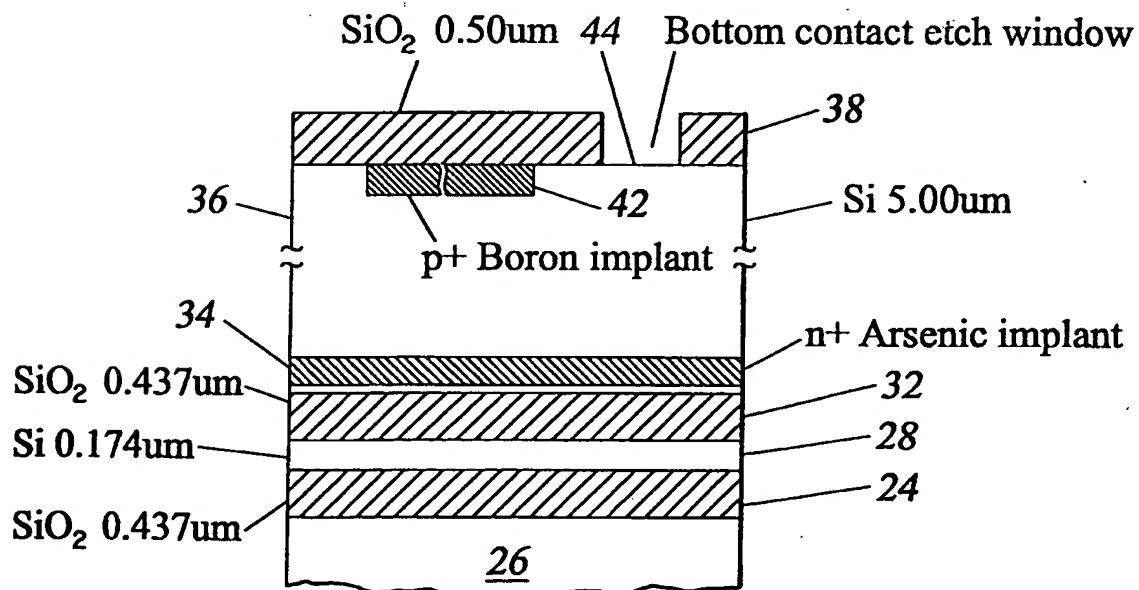


FIG. 13

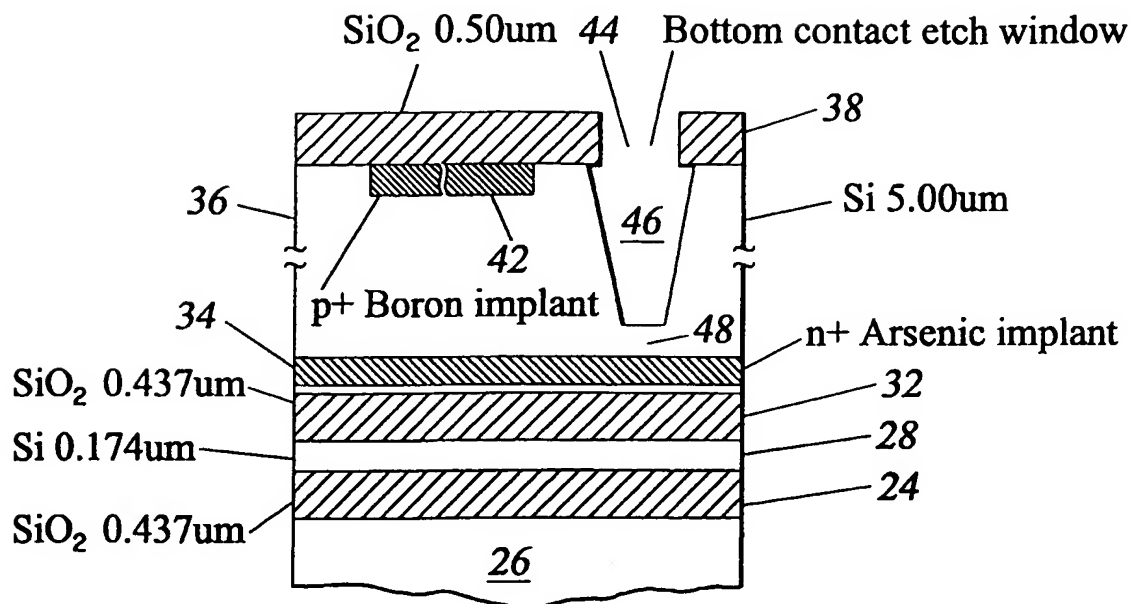
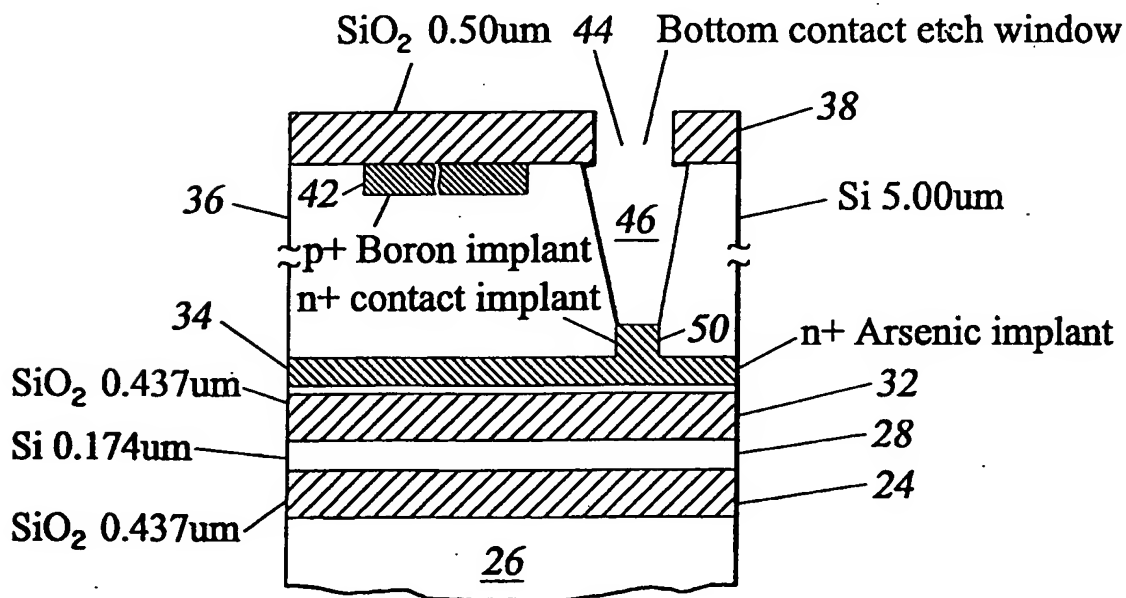
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**FIG. 14****FIG. 15**

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**FIG. 16****FIG. 17**

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**FIG. 18****FIG. 19**

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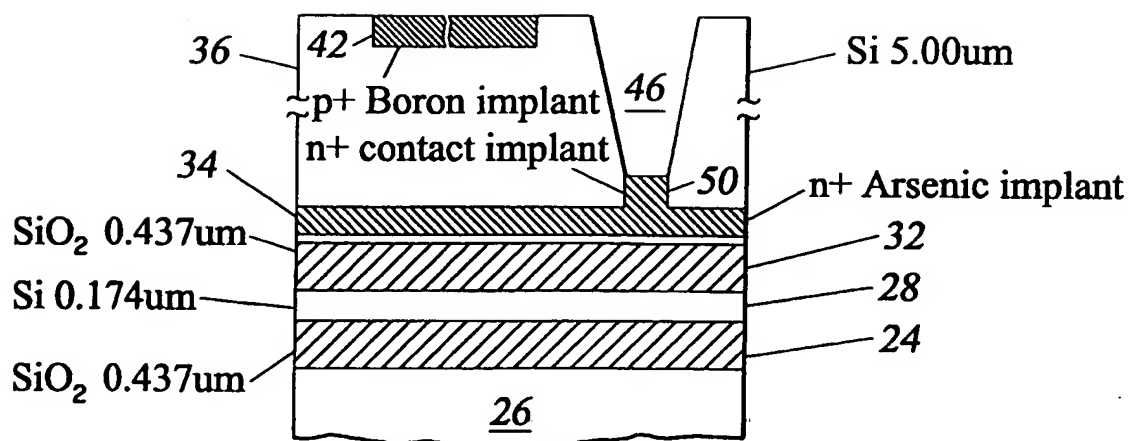


FIG. 20

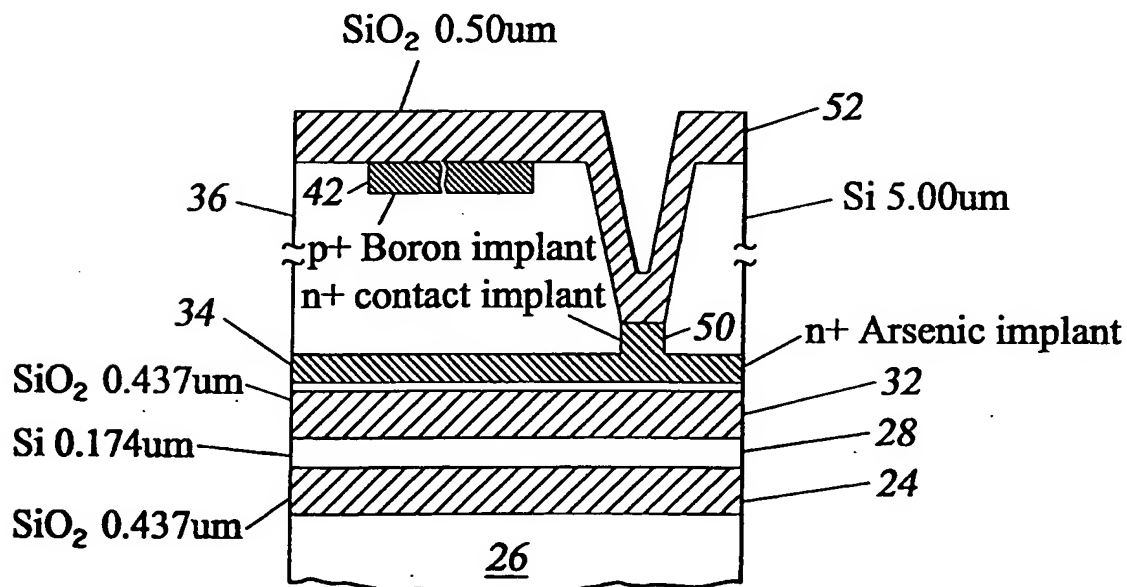
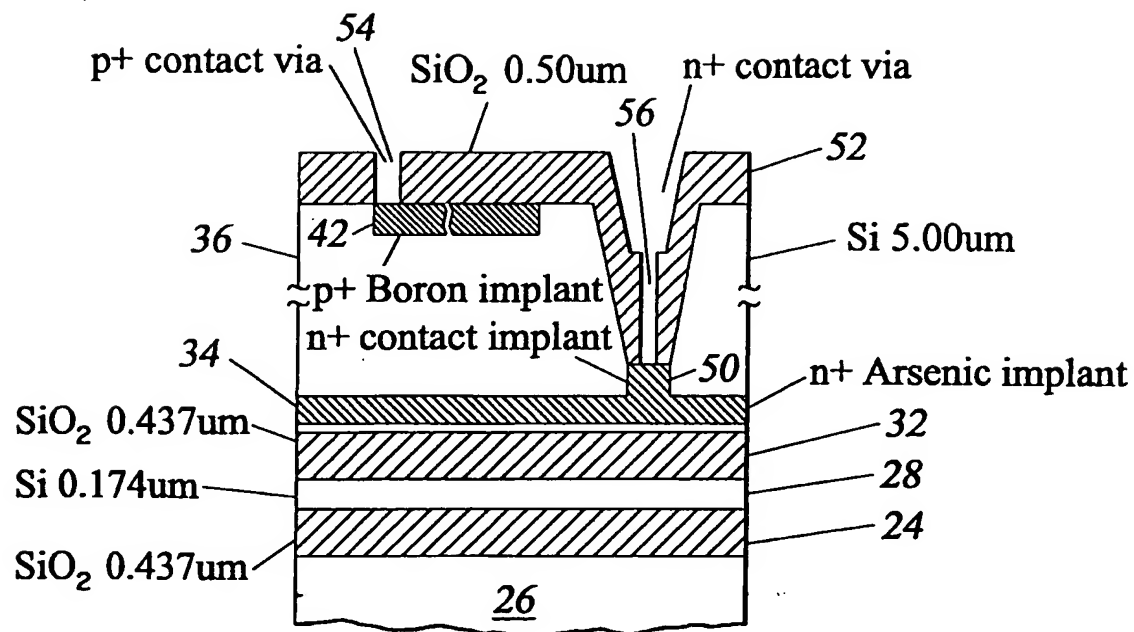
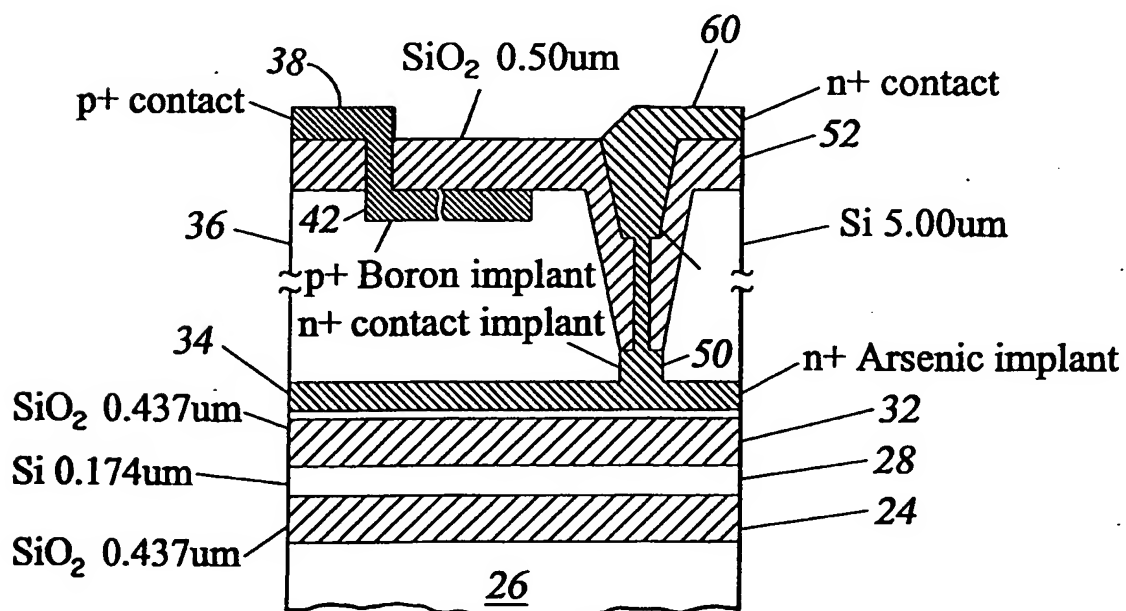
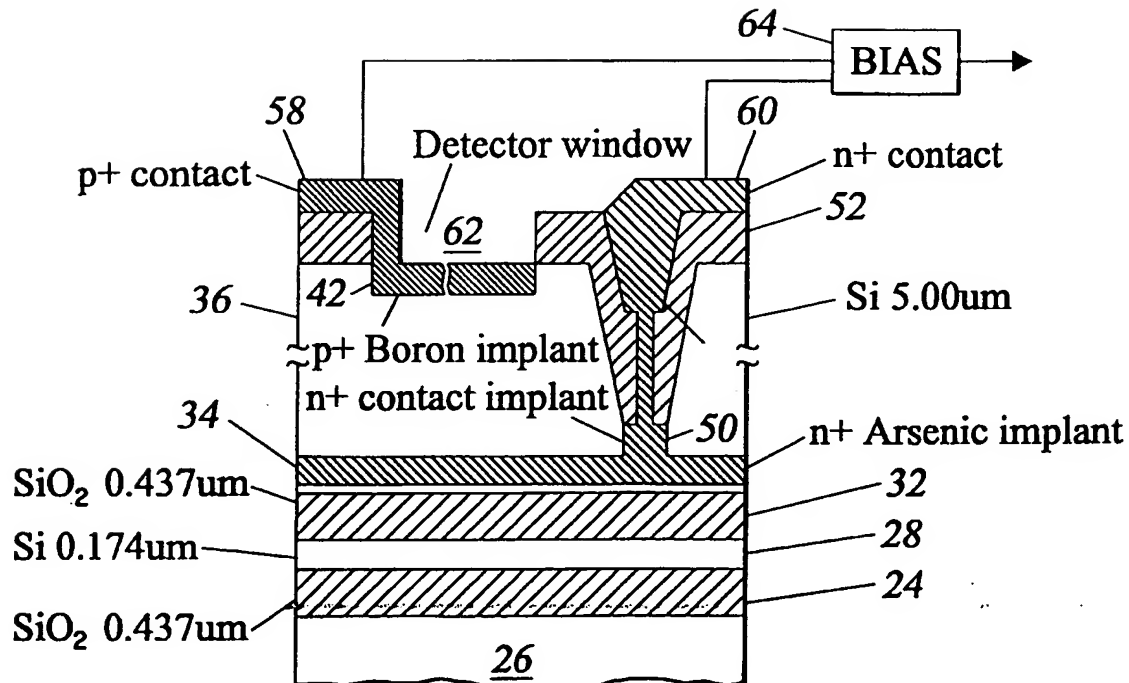
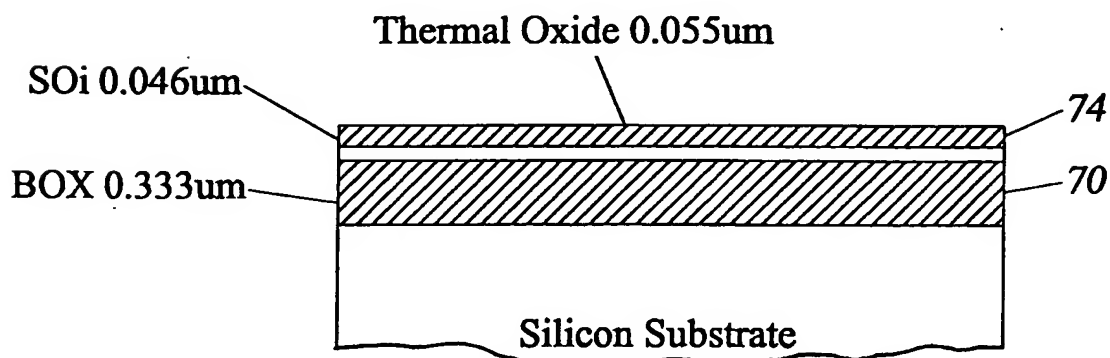


FIG. 21

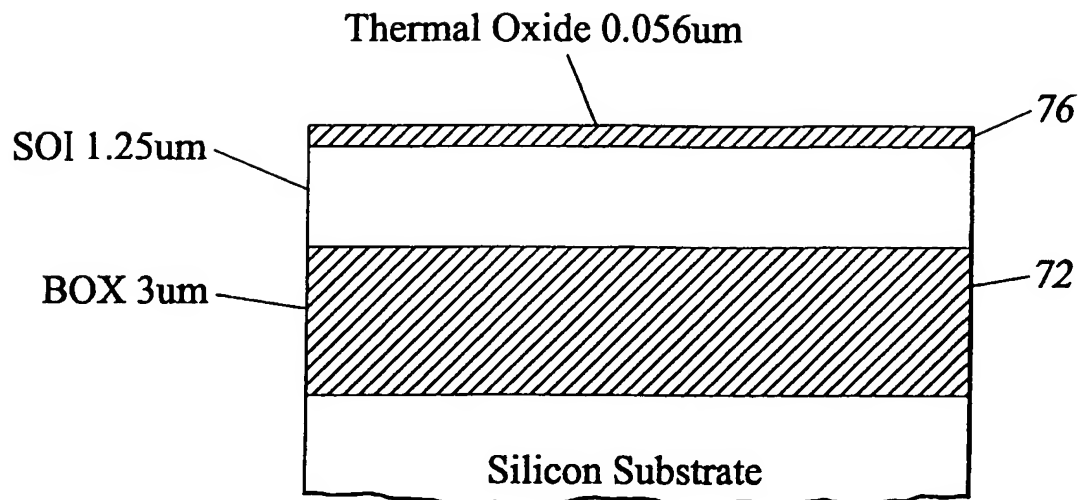
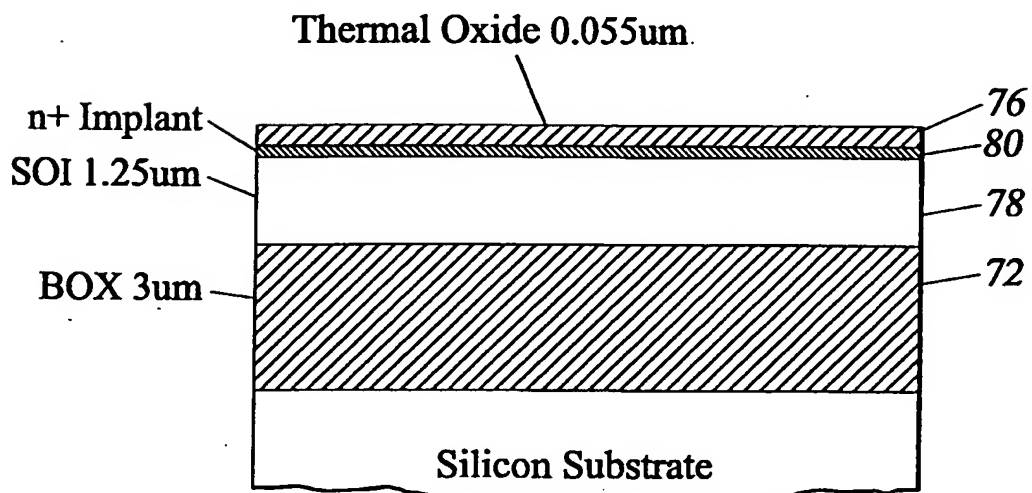
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**FIG. 22****FIG. 23**

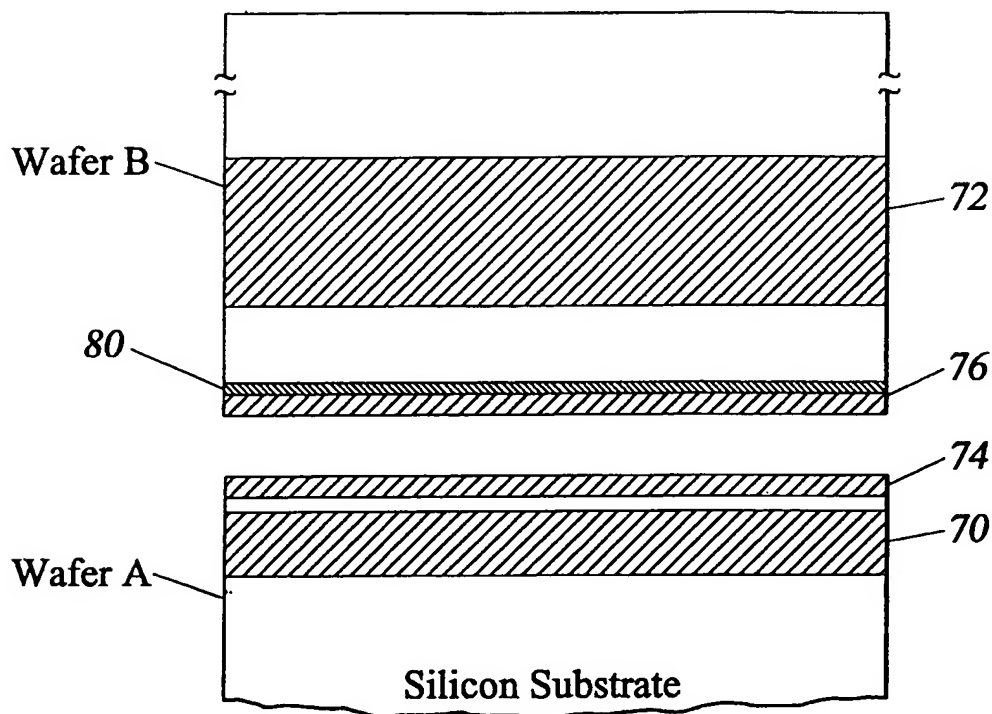
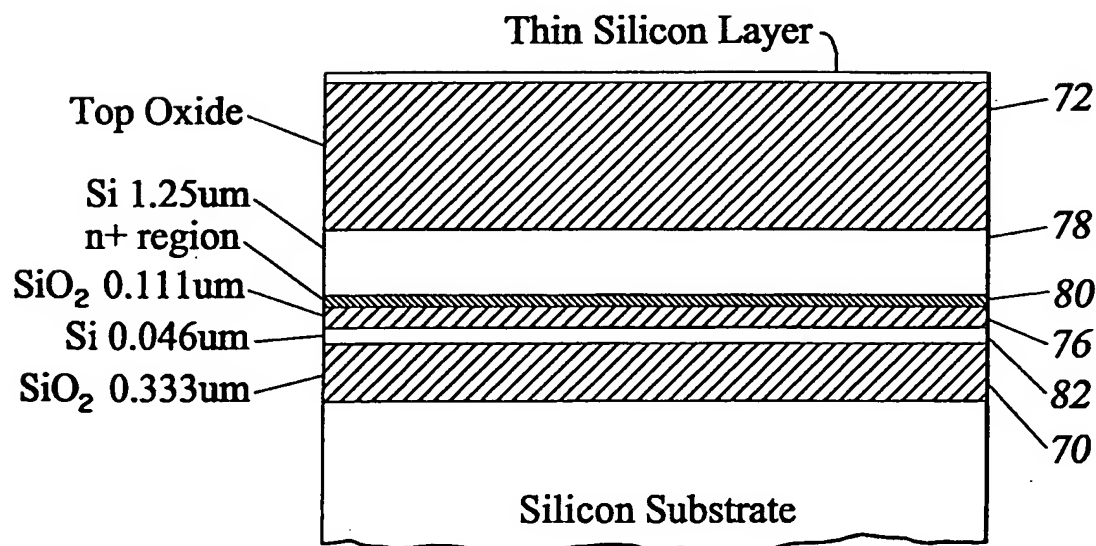
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*FIG. 24**FIG. 25*

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**FIG. 26****FIG. 27**

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**FIG. 28****FIG. 29**

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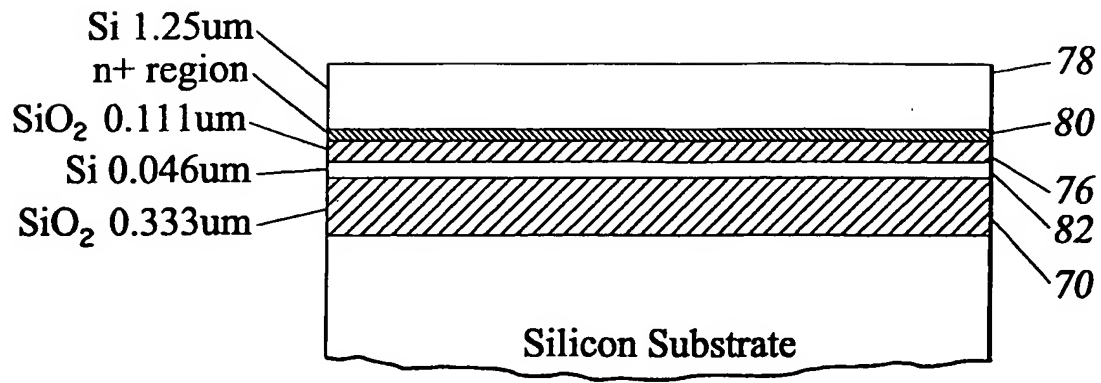


FIG. 30

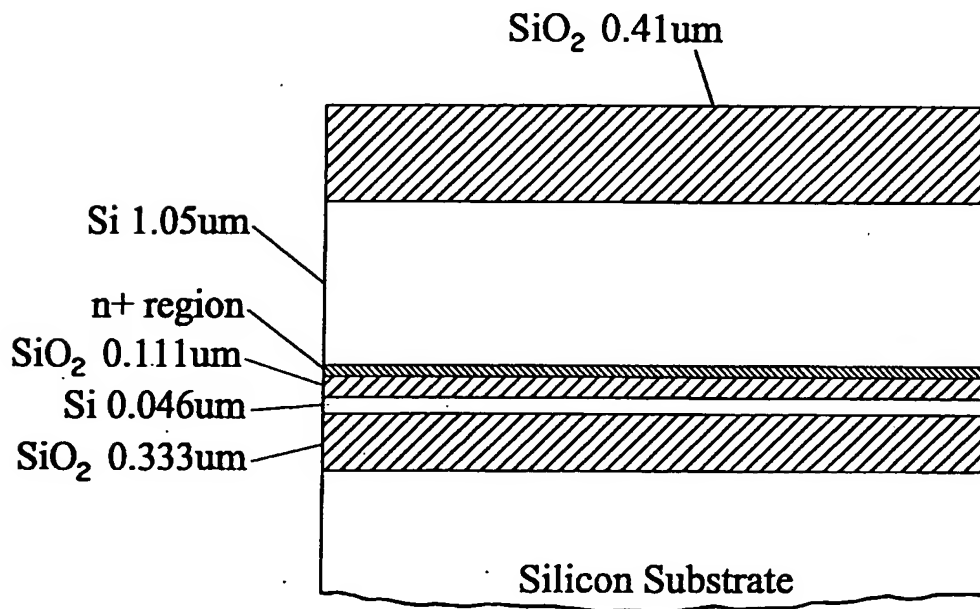
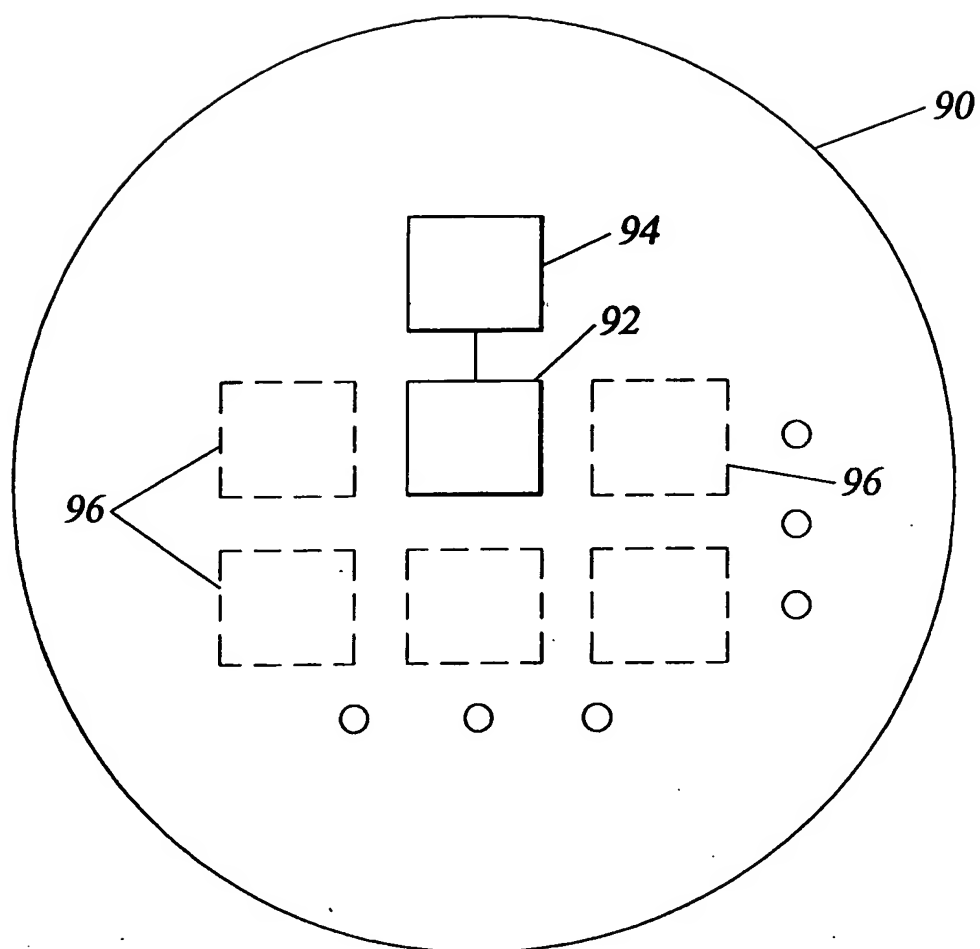


FIG. 31

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**FIG. 32**